

FIG. 1

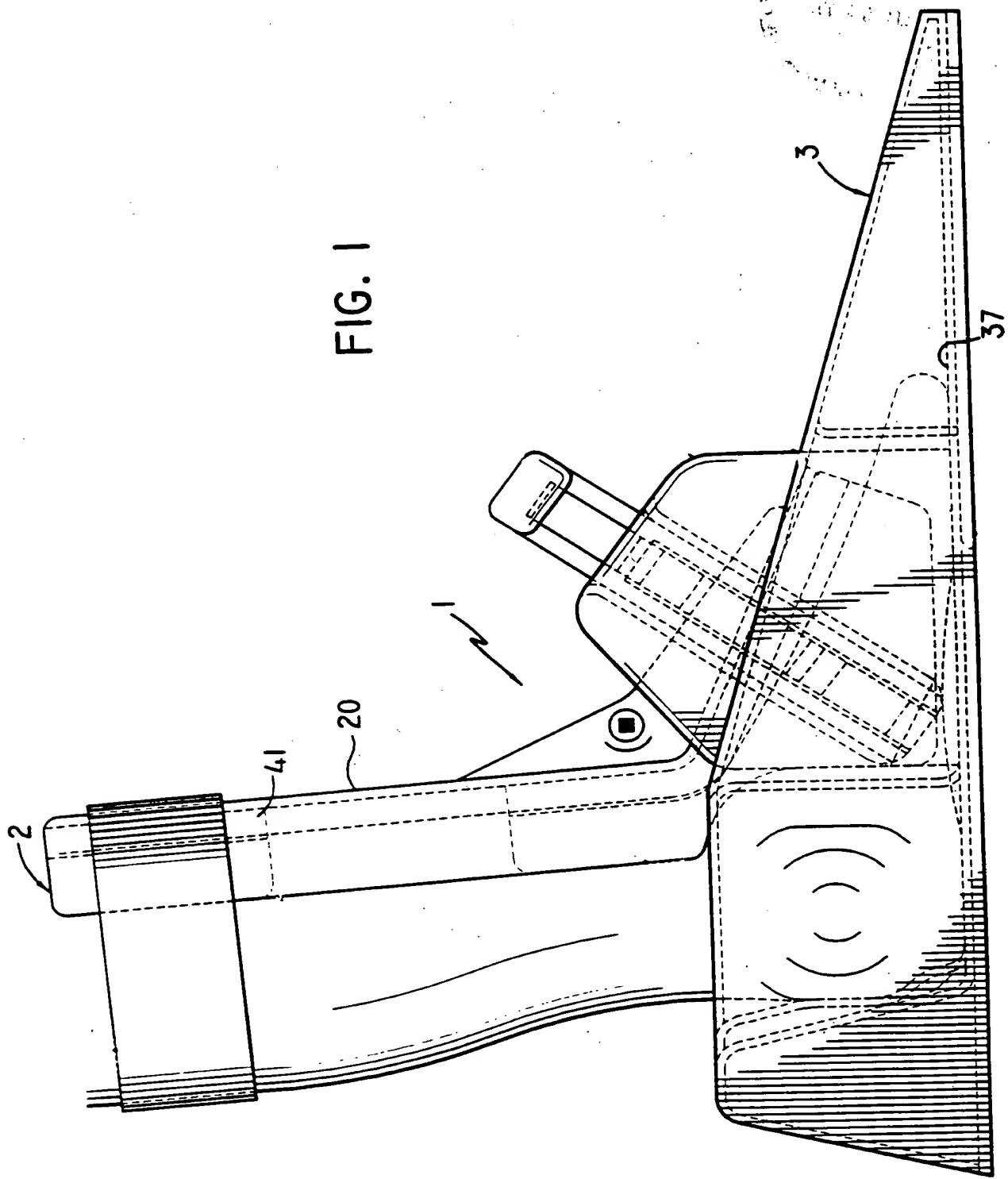
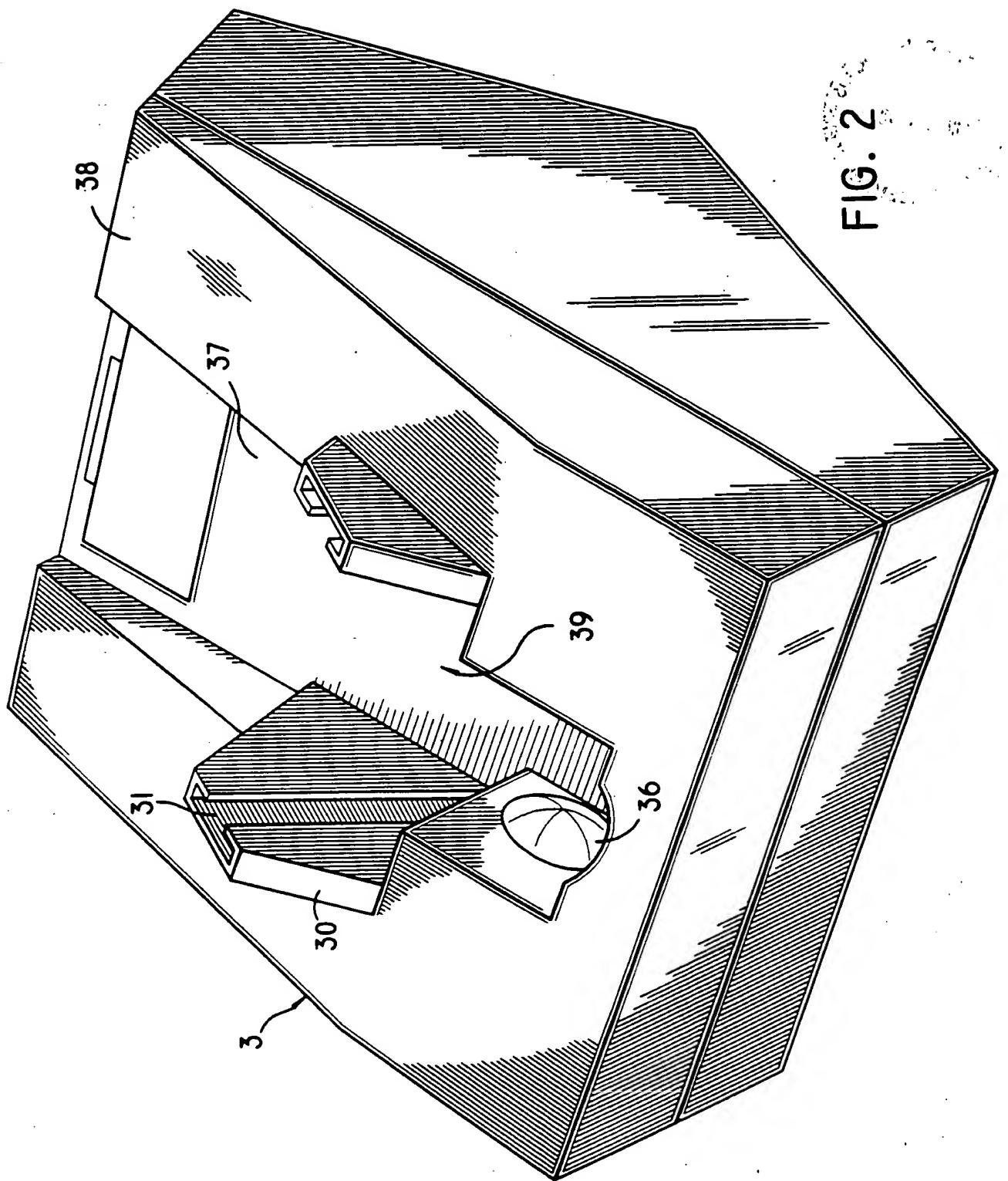


FIG. 2



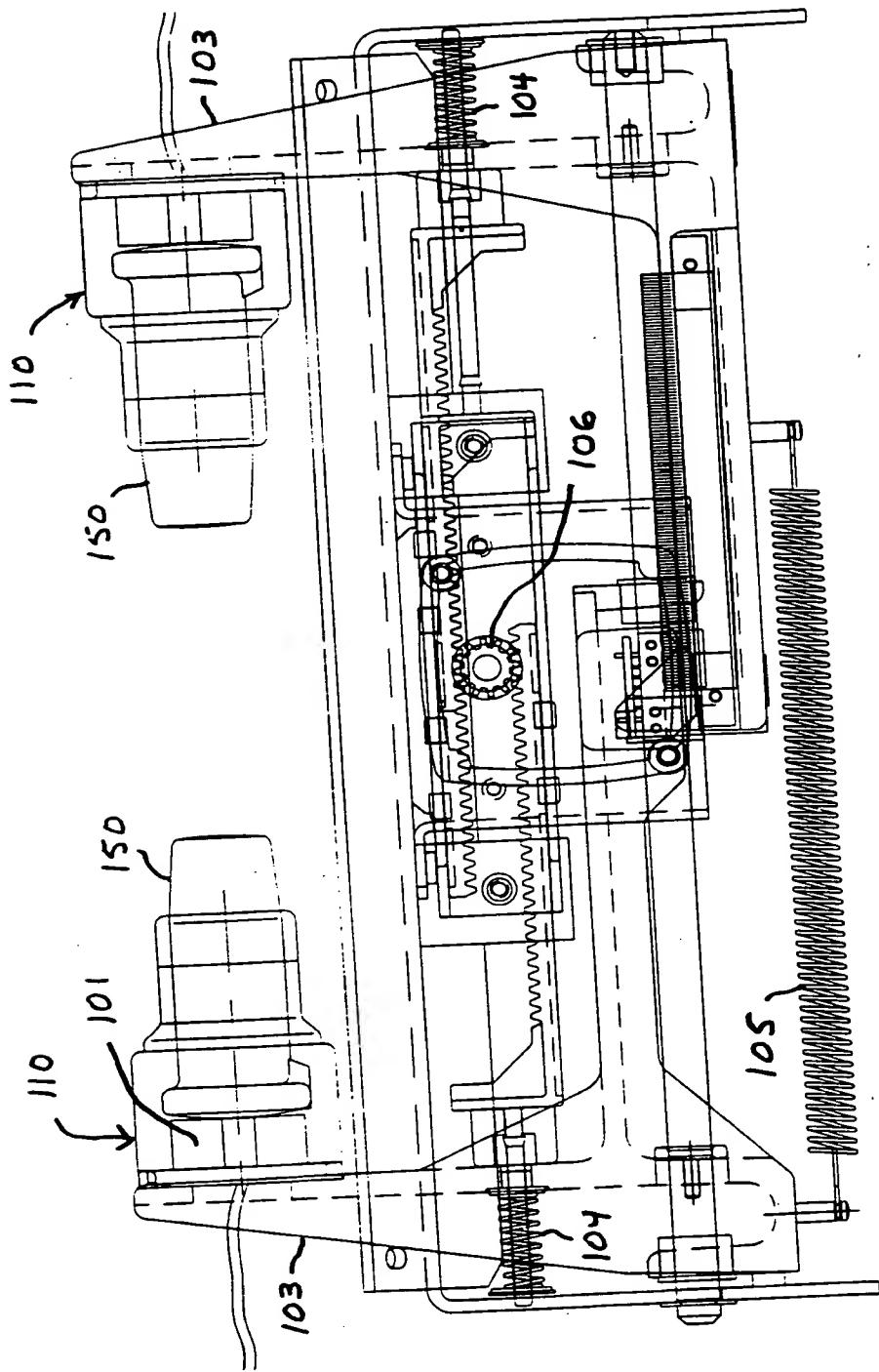


FIG. 3

FIG. 4A

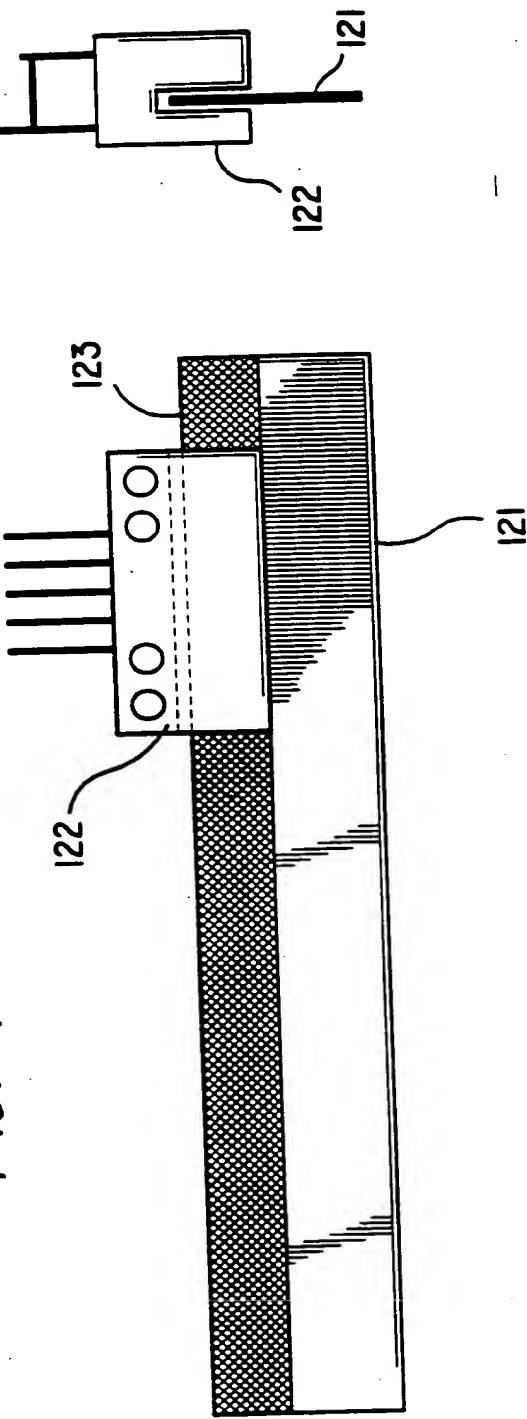


FIG. 4B

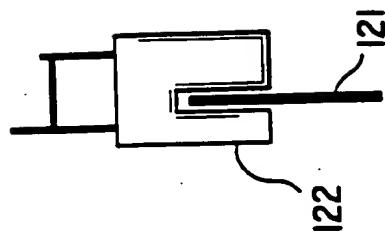
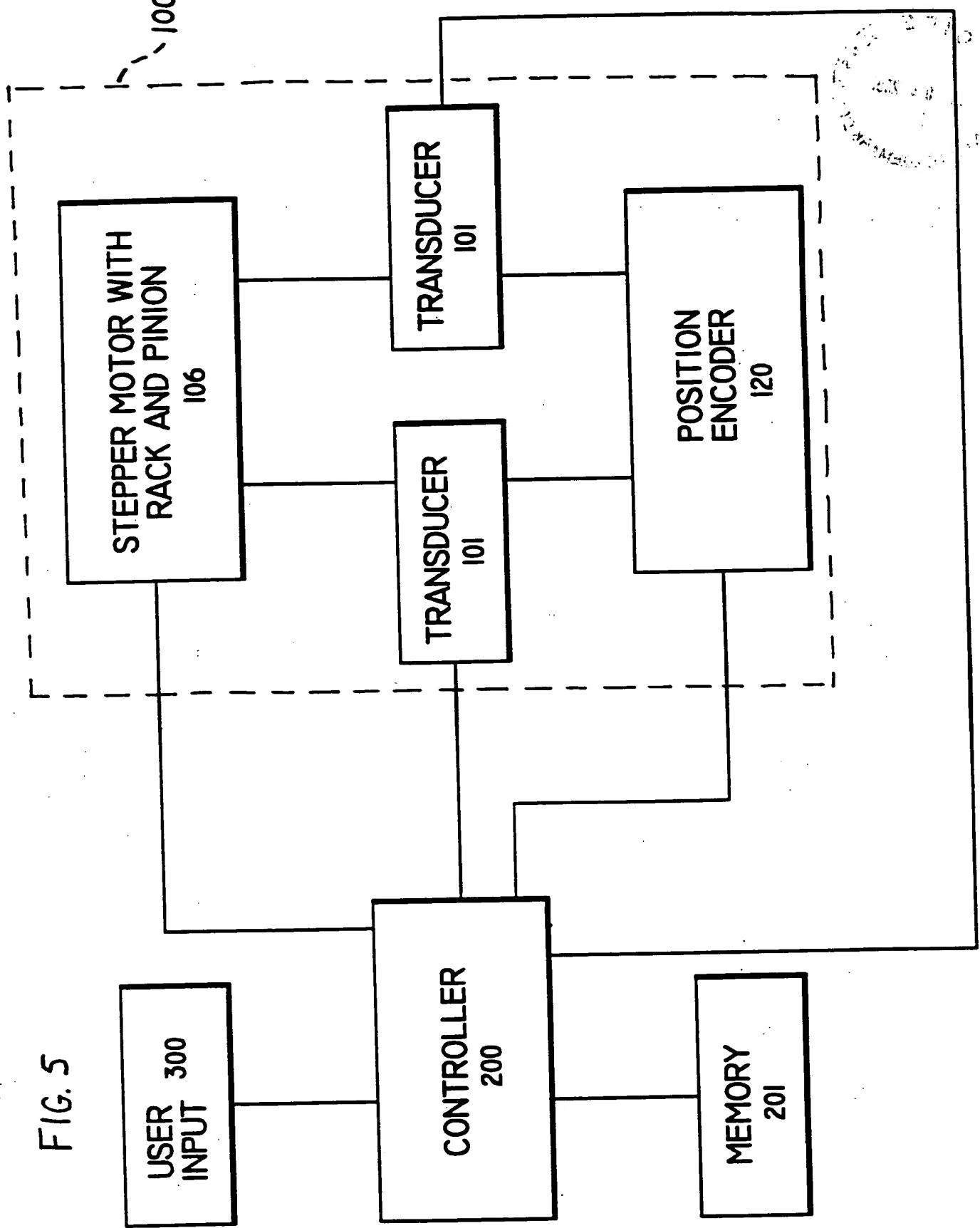


FIG. 5



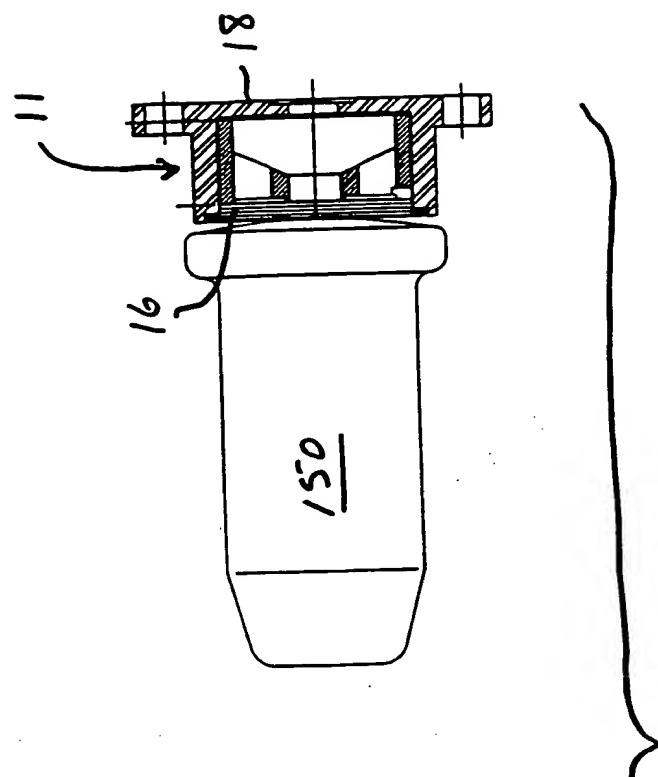
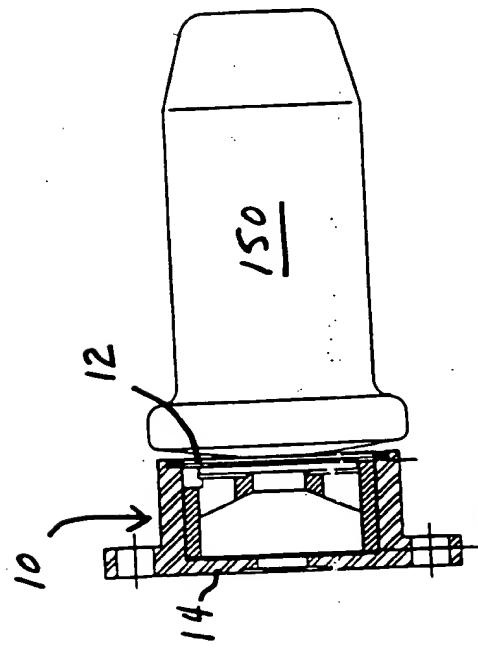


FIG. 6



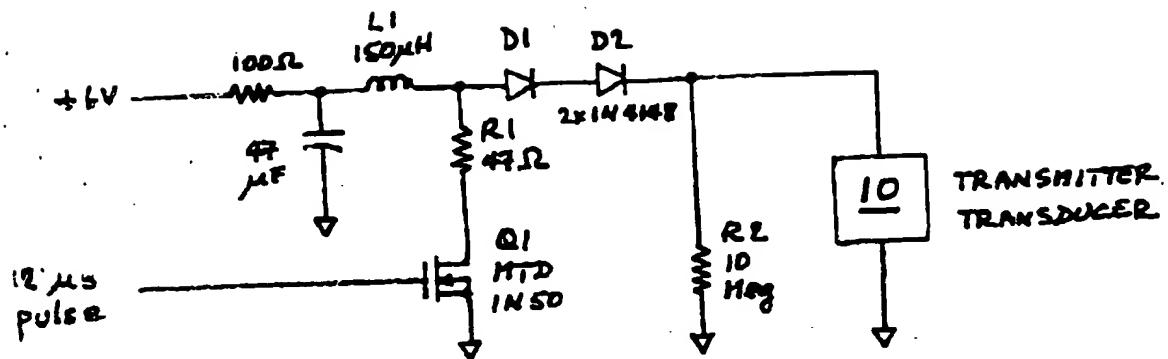


FIG. 7A

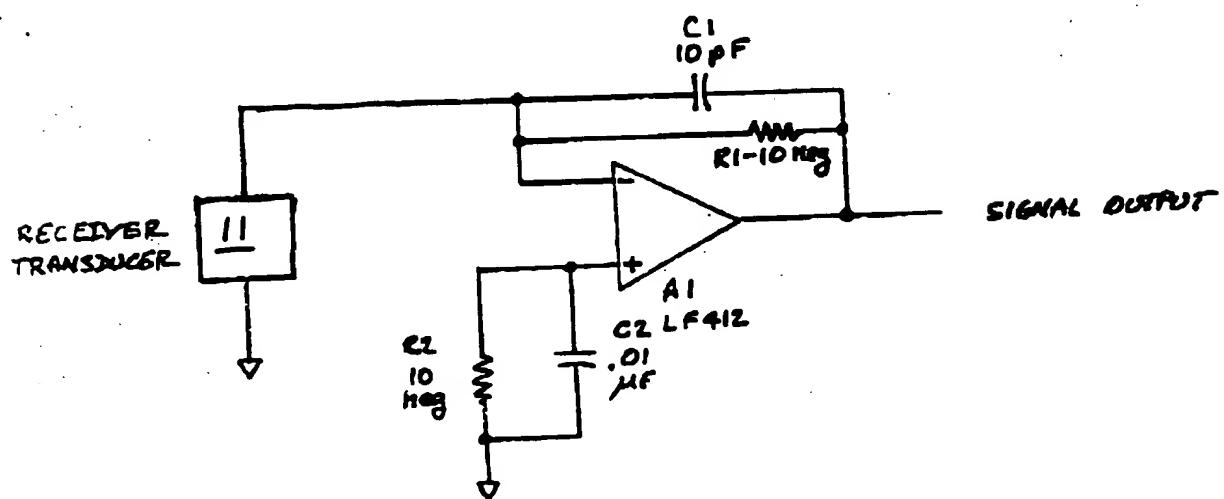
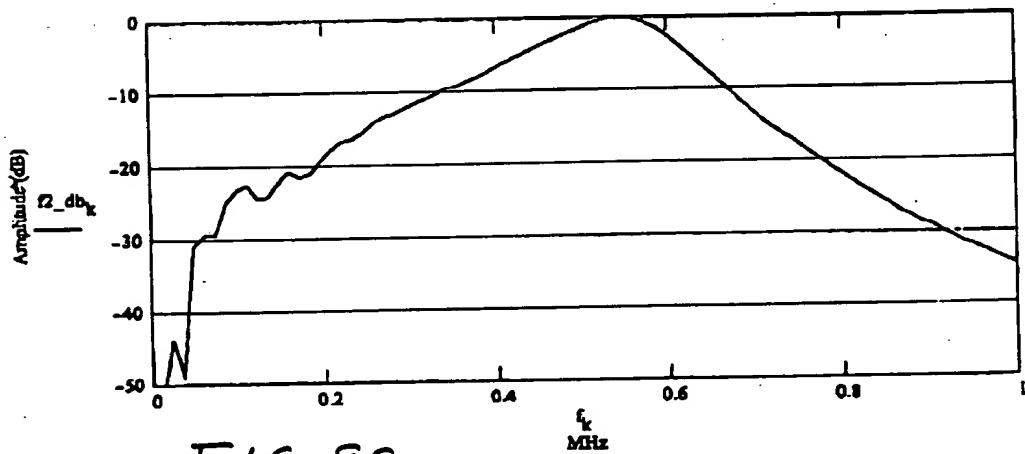
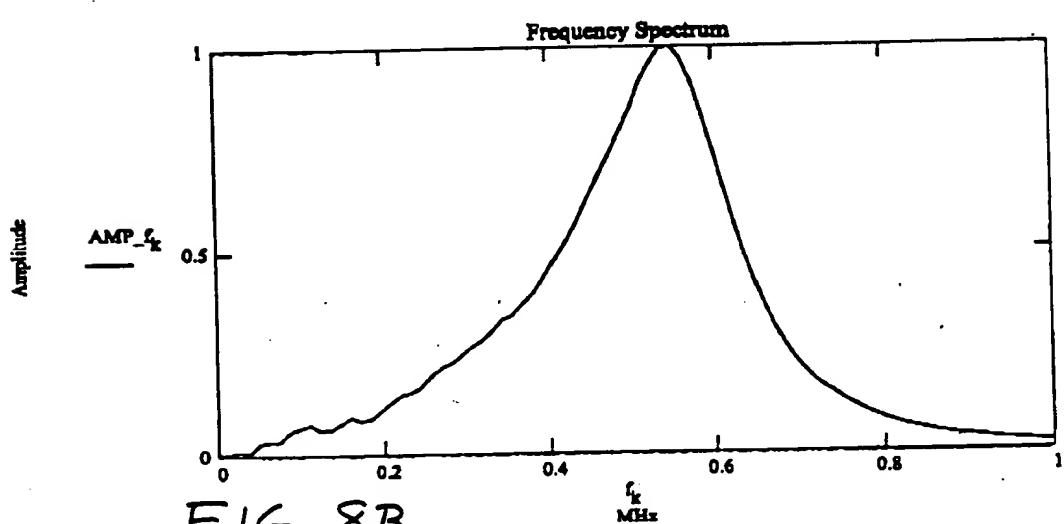
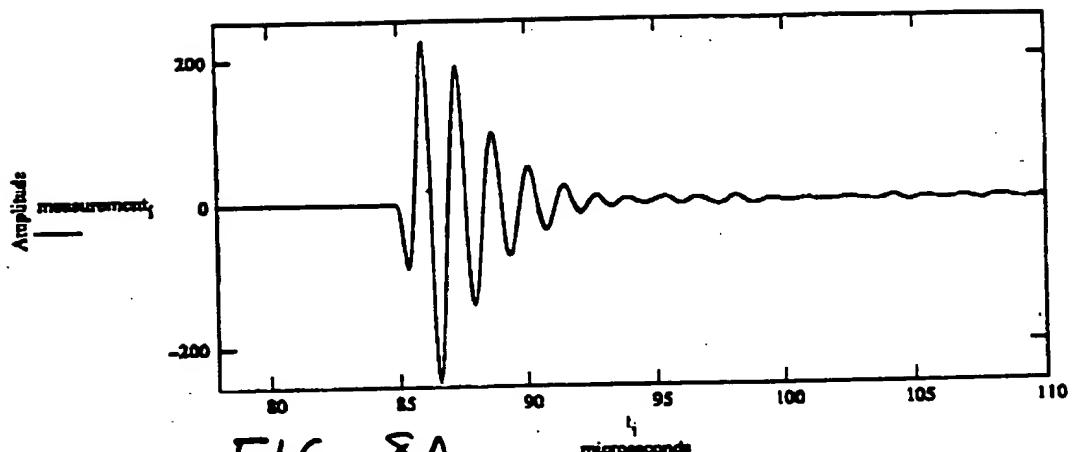


FIG. 7B



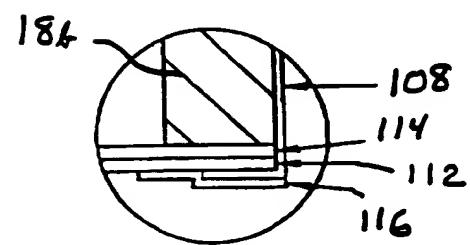
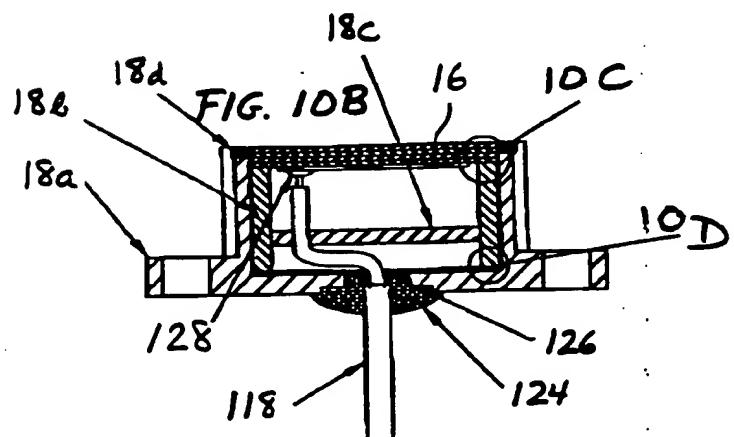
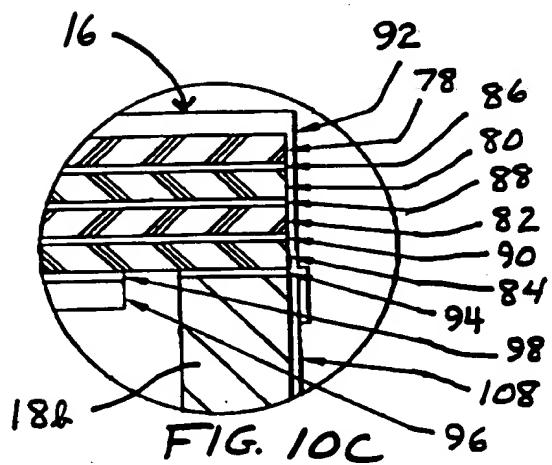
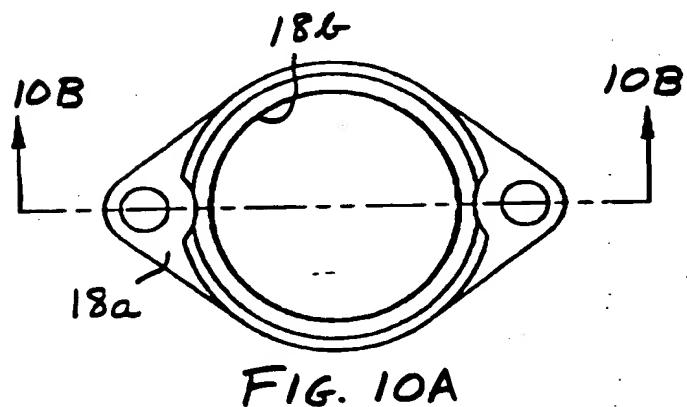
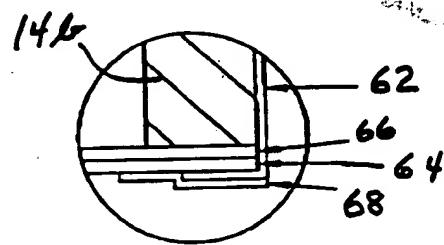
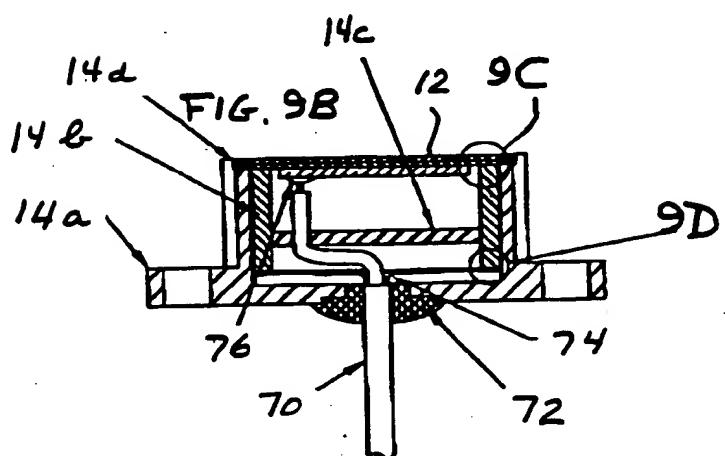
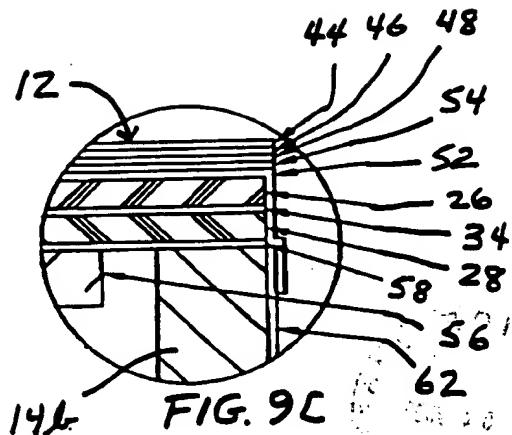
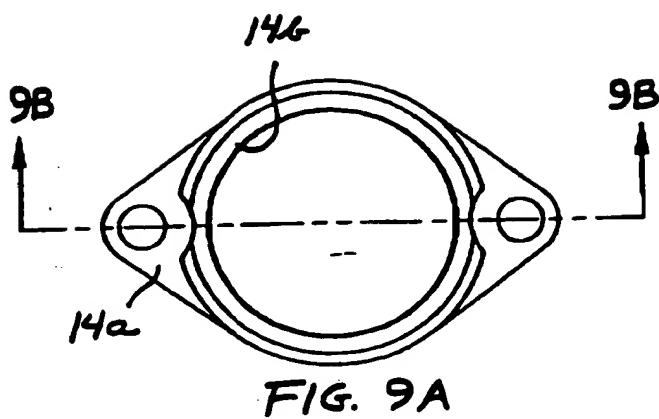


FIG. 13

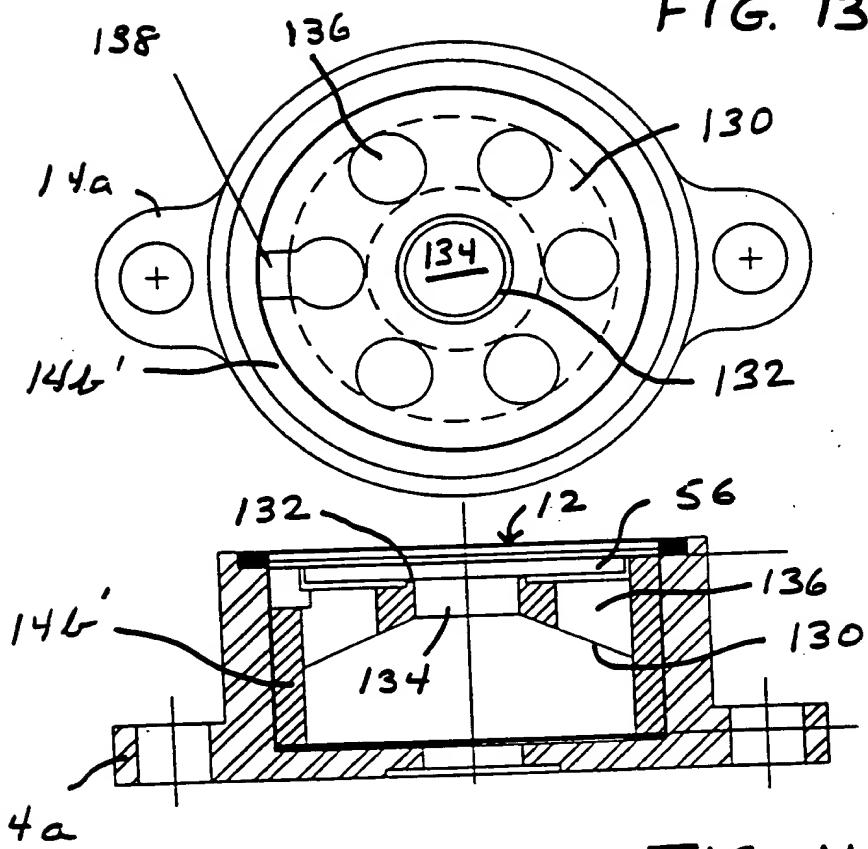


FIG. 11

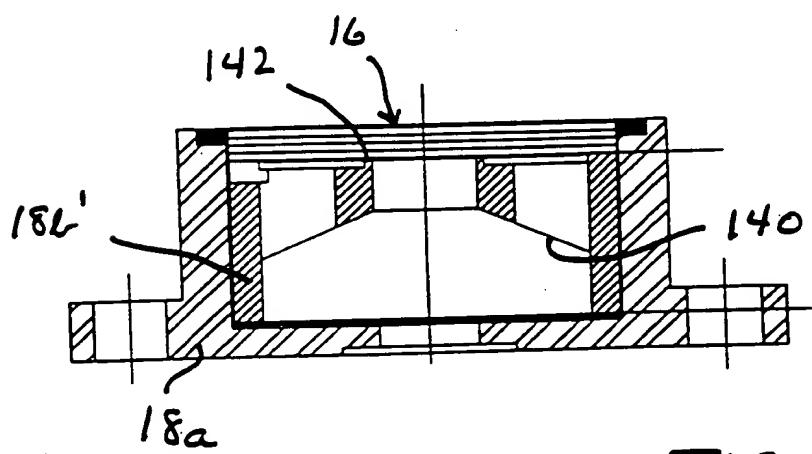


FIG. 12

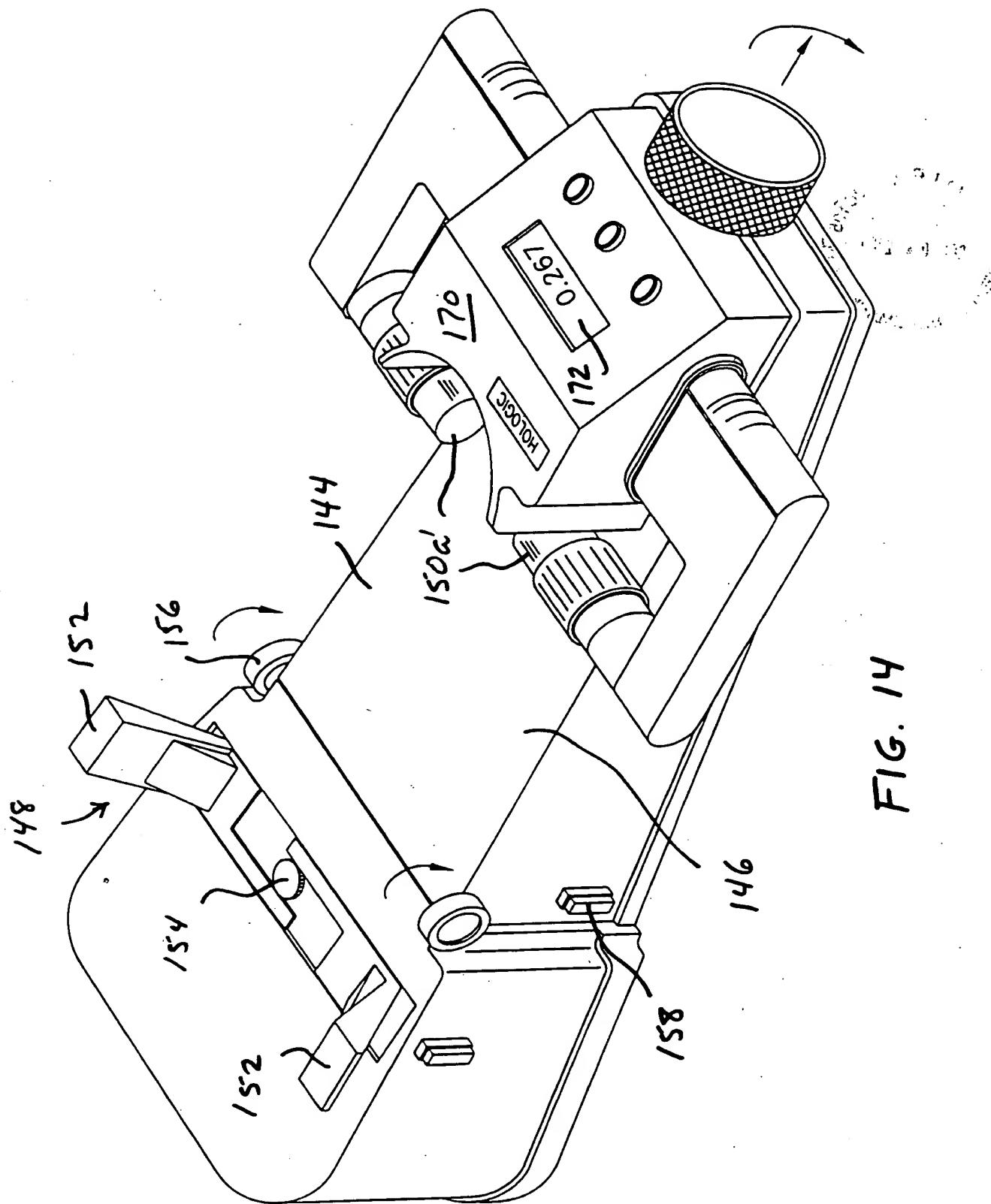


FIG. 14

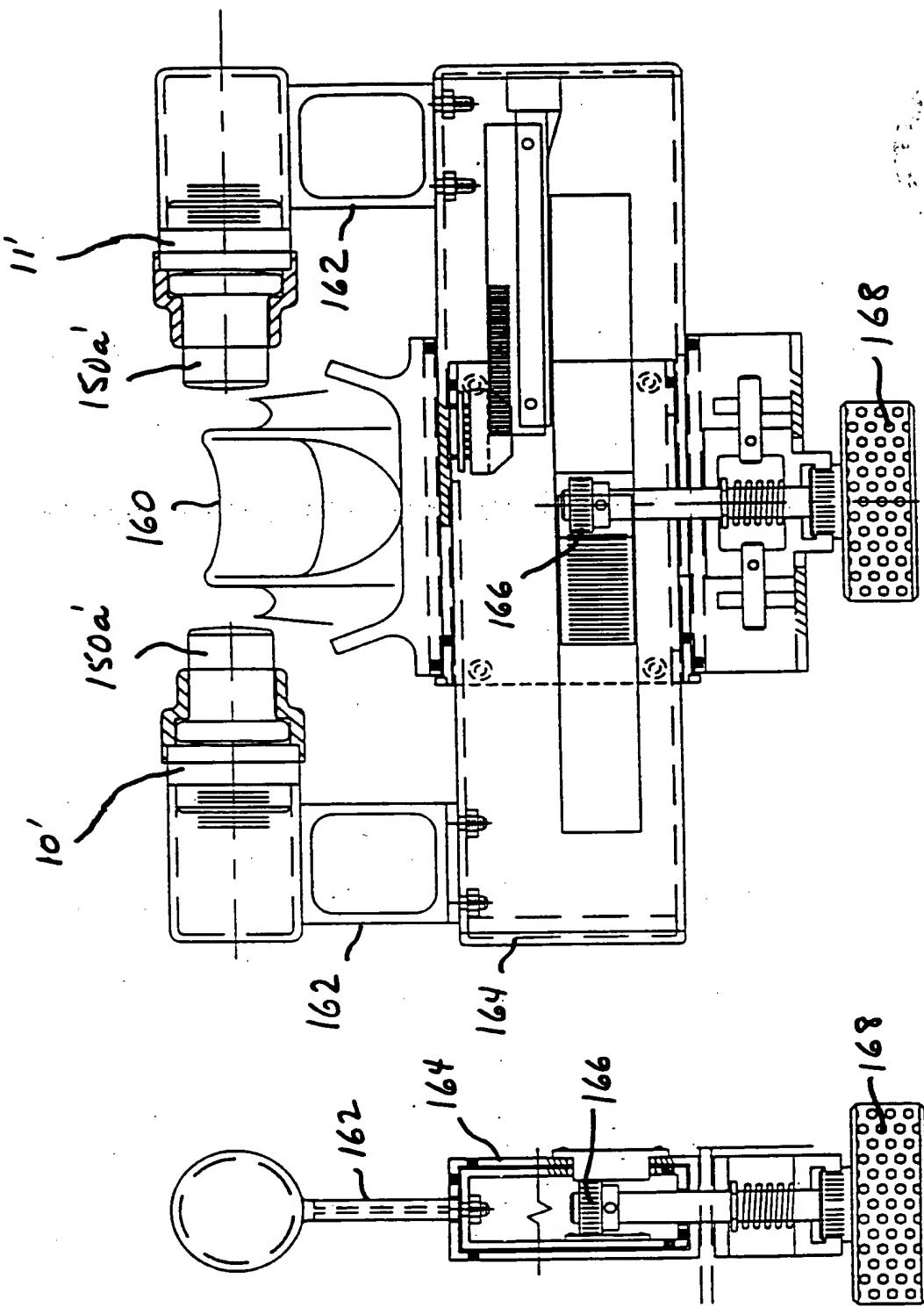
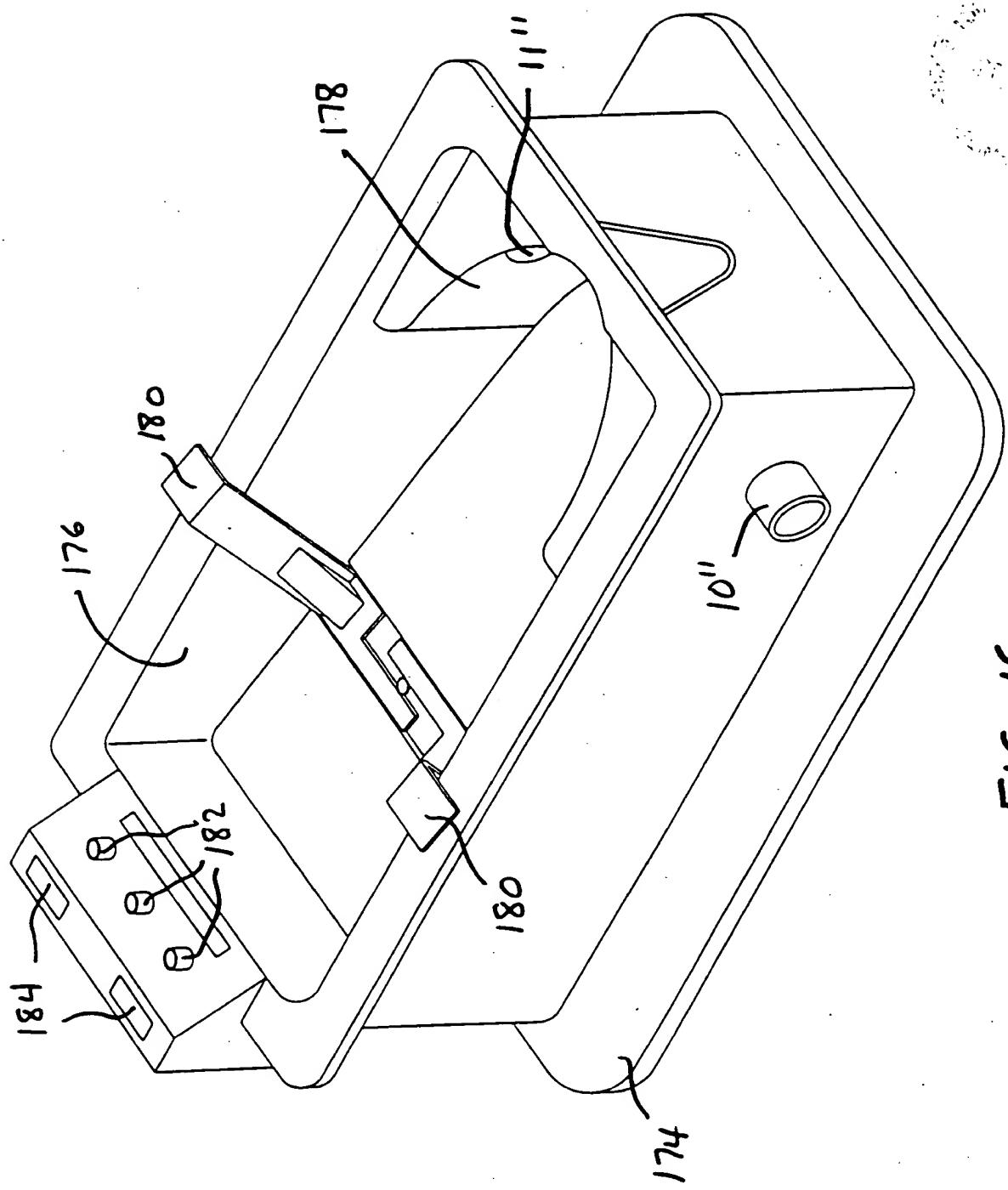


FIG. 15A

FIG. 15B

FIG. 16



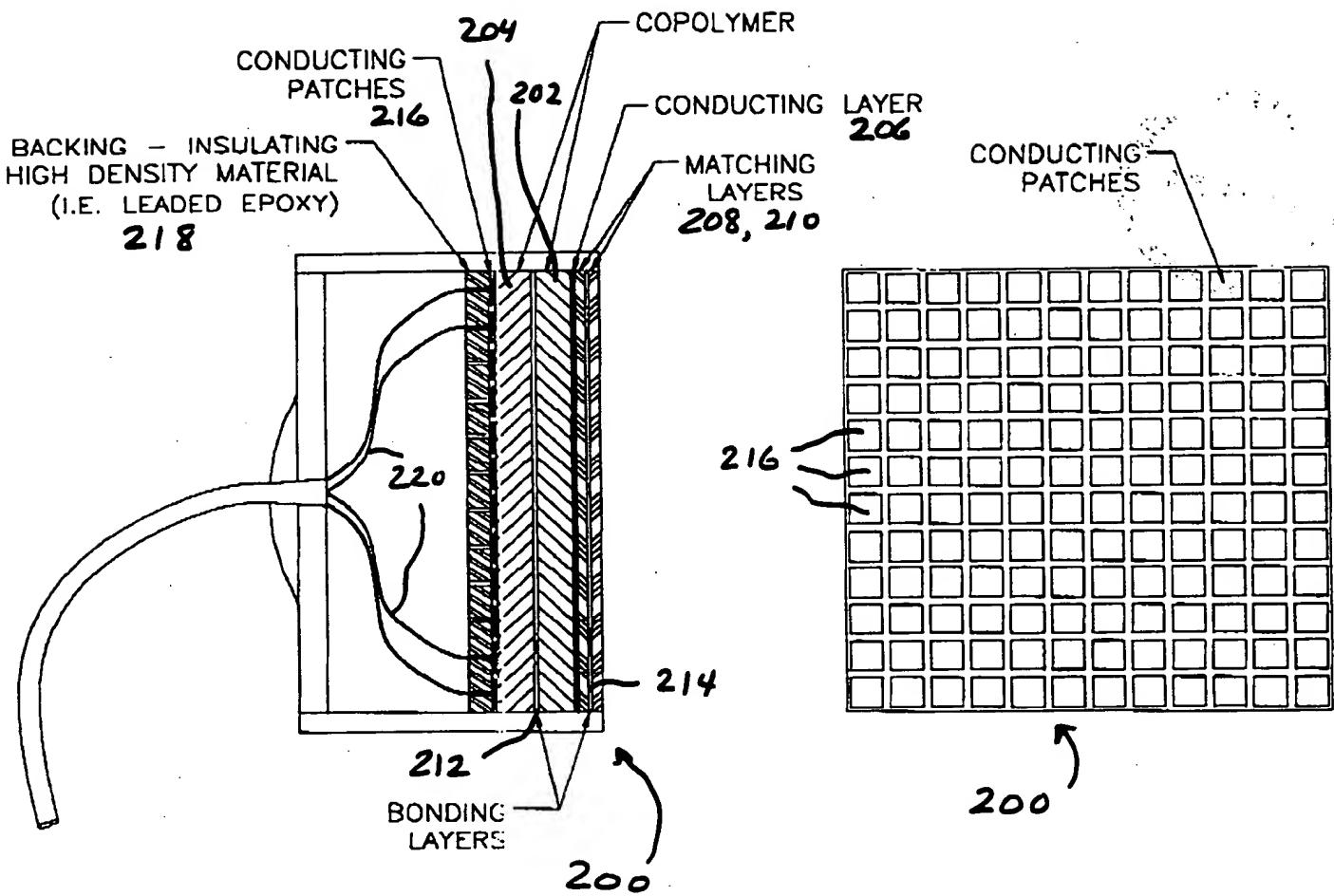


FIG. 17B

FIG. 17A

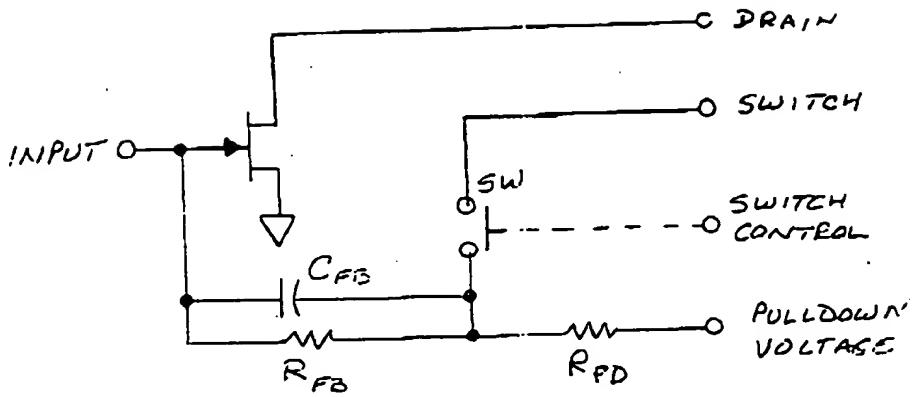


FIG. 18A N-Channel FET Input Stage

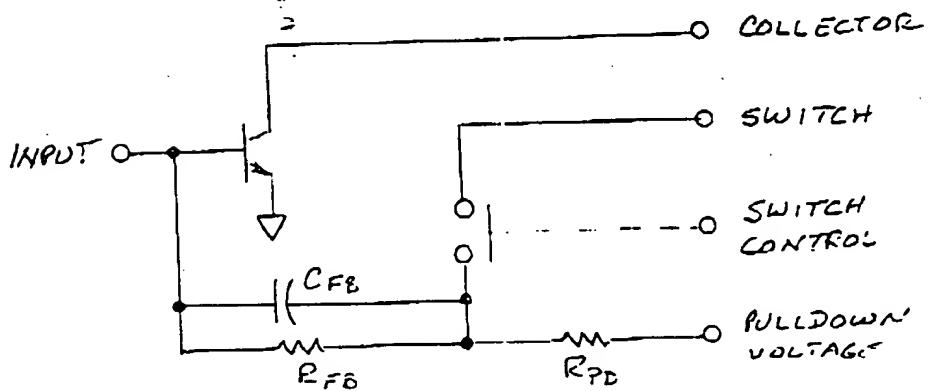


FIG 18B NPN Transistor Input Stage

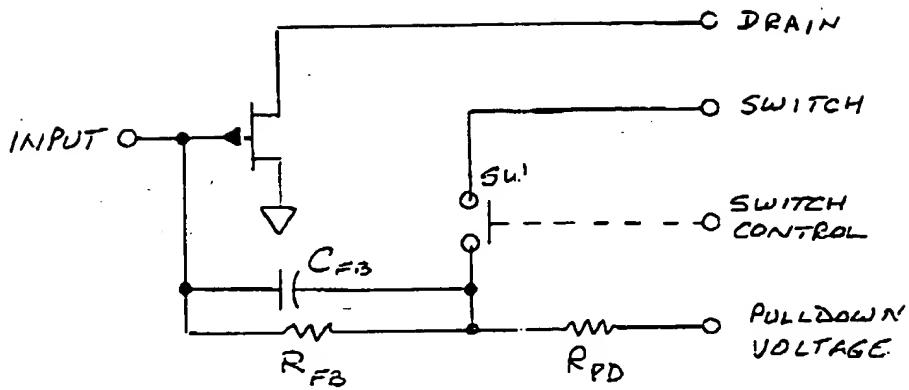


FIG. 18C - P-Channel FET Input Stage

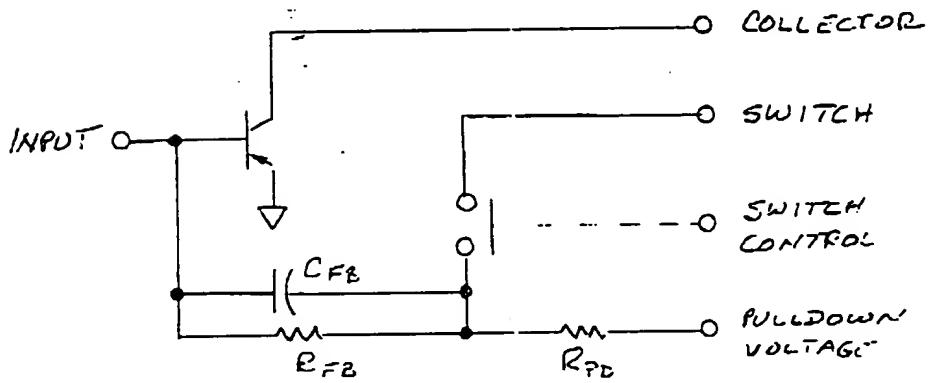
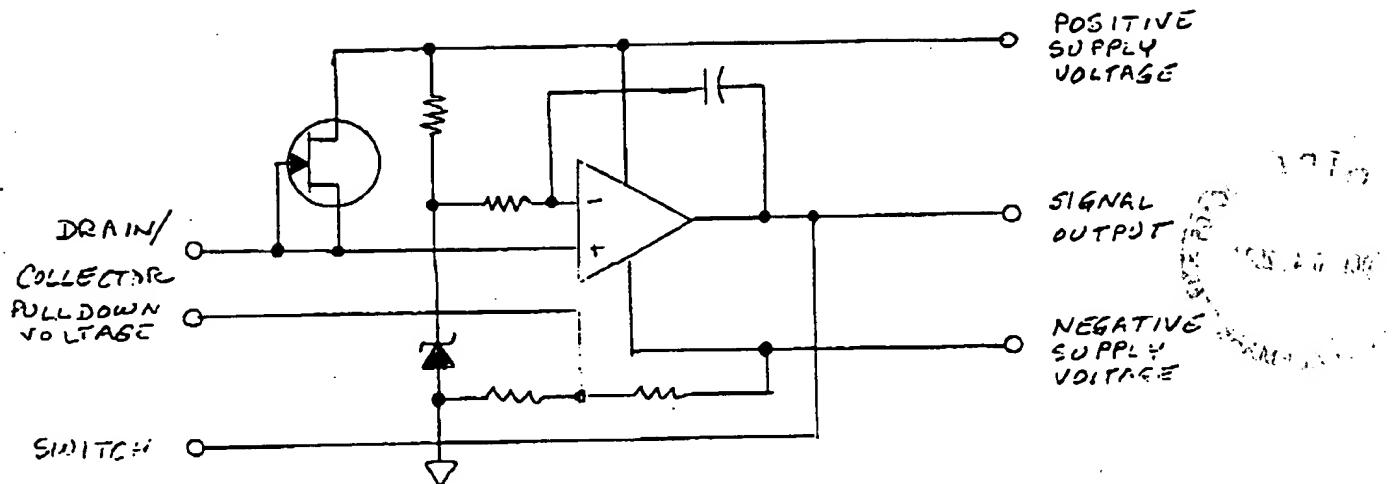
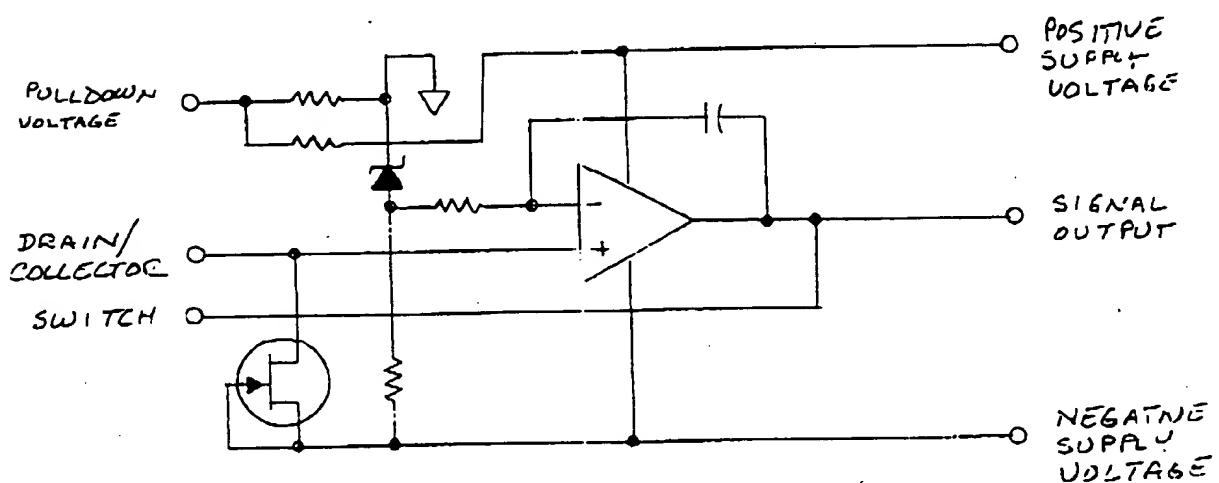


FIG 18D - PNP Transistor Input Stage



**FIG 18E - PREAMPLIFIER OUTPUT STAGE
FOR N-CHANNEL OR NPN INPUT STAGE**



**FIG.18F - PREAMPLIFIER OUTPUT STAGE
FOR P-CHANNEL OR PNP INPUT STAGE**